WHAT IS CLAIMED IS:

1. A system for taking at least one software program written in a high level language and generating an instruction set architecture optimized for executing that program(s).

2. The system of claim 1, wherein:

the instruction set architecture is represented as a set of configurations containing one or more extension instructions to instructions in an existing standard or existing user defined instruction set architecture; and

the extension instructions operate on pre-existing or automatically generated states and register files.

3. The system of claim 2, wherein the extension instructions contain vectorized versions of the existing instructions.

4. The system of claim 2, wherein the extension instructions contain VLIW combinations of the existing instructions.

5. The system of claim 2, wherein the extension instructions contain fused combinations of the existing instructions.

6. The system of claim 2, wherein the extension instructions contain specialized versions of the existing instructions.

7. The system of claim 2, wherein the extensions contain vectorized versions of operations supported by the high level language.

8. The system of claim 2, wherein the extension instructions contain VLIW combinations of operations supported by the high level language.

9. The system of claim 2, wherein the extension instructions contain fused combinations of operations supported by the high level language.

10. The system of claim 2, wherein the extension instructions contain specialized versions of operations supported by the high level language.

11. The system of claim 2, wherein the extension instructions contain at least two of vectorized, VLIW, fused and specialized versions of the existing instructions.

12. The system of claim 2, wherein the extension instructions contain at least two of vectorized, VLIW, fused and specialized versions of operations supported by the high level language.

13. The system of claim 2, wherein one or more of the extension instructions are vectorized, VLIW, fused or specialized versions of other user defined instructions described using an extension language.

14. The system of claim 2, wherein:

instruction set architecture generation is guided by analysis information gathered from at least one software program; and

the analysis information is gathered for each region of code that could get a performance improvement from a generated instruction set algorithm.

15. The system of claim 14, wherein the analysis information includes an execution count of each region as determined from real or estimated profiling information.

16. The system of claim 14, wherein the analysis information includes an execution count of each region as determined from user-supplied directives.

17. The system of claim 14, where the analysis information includes a dependence graph of each region.

18. The system of claim 14, where the analysis information includes a set of operation vector lengths that can be used to improve performance of each region.

19. The system of claim 14, wherein each region is evaluated with a set of instruction set architecture configurations to determine a performance improvement that would result if instructions, operations, register files, and states represented by the configuration could be used for the region.

20. The system of claim 19, wherein:

instruction set architecture generation is guided by an estimate of hardware cost of each instruction set architecture configuration that includes a cost of logic necessary to implement instructions, operations, register files, and state represented by the configuration; and

the hardware cost and performance improvement of each instruction set architecture configuration for each region is used to determine a set of instruction set architecture configurations that together describe the generated instruction set architecture such that the performance improvement of the software program(s) is increased as much as possible while the hardware cost of the generated instruction set architecture does not exceed a cost budget.

21. The system of claim 19, wherein:

instruction set architecture generation is guided by an estimate of hardware cost of each instruction set architecture configuration that includes a cost of logic necessary to implement instructions, operations, register files, and state represented by the configuration; and

the hardware cost and performance improvement of each instruction set architecture configuration for each region is used to determine the set of instruction set architecture configurations that together describe the generated instruction set architecture such that the hardware cost of the generated instruction set architecture is as small as possible while providing a performance improvement that is greater or equal to a performance goal.

22. The system of claim 19, wherein the hardware cost and performance improvement of each instruction set architecture hardware configuration for each region is used to

determine the set of instruction set architecture configurations that together describe the generated instruction set architecture such that the hardware cost of the generated instruction set architecture is smaller than a predetermined function of the performance improvement.

23. The system of claim 19, wherein a performance improvement provided by a particular instruction set architecture configuration for a particular region is determined by an instruction scheduling algorithm operating on a modified dependence graph of the region.

24. The system of claim 23, wherein the dependence graph is modified to replicate operations with an operation width that is less than one.

25. The system of claim 23, wherein the dependence graph is modified to replace groups of operations with a single fused operation.

26. The system of claim 19, wherein the performance improvement provided by a particular instruction set architecture configuration for a particular region is determined using resource limits.

27. The system of claim 2, wherein instruction set architecture generation is guided by an estimate of hardware cost of each instruction set architecture configuration that includes a cost of logic necessary to implement instructions, operations, register files, and state represented by the configuration.

28. The system of claim 27, wherein the hardware cost is estimated by adding hardware costs of components present in the instruction set architecture configuration.

29. The system of claim 27, wherein the hardware cost is reduced to represent reduced logic necessary when specialized operations replace generic operations.

30. A system for taking at least one software program written in a high level language and generating an instruction set architecture optimized for executing said at least one program, by adding one or more new instructions based on the analysis of the said at least one program.

31. A system for taking at least one software program written in a high level language and generating an instruction set architecture optimized for executing said at least one program, by adding one or more new register files based on the analysis of the said at least one program.